Design and Implementation of Modified Multilevel Sepic Converter for PV Applications

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Abstract

Abstract-In this manuscript, a DC-DC converter of modified multilevel sepic model with single switch is proposed here. The designed converter combines the voltage tripler circuit, which improves the voltage ratio and reduces the ripple source of the scheme. Another merit of the designed converter is reduces the voltage strain and utilized for PV based applications. The functioning of the designed model in Continuous-Conduction Mode (CCM)is discussed. The converter boosts the 30 V of PV input to 400 V output voltages. The efficiency attained by the designed converter is 94%. The Theoretical examination of the designed converter is presented and it is done with MATLAB simulink. To analyse the performance of this DC-DC converter a model was developed and tested. From the investigational results obtained, it is analysed that the designed converter performs better and suitable for PV based application.

KEYWORDS: High voltage conversion, irradiation, multilevel sepic converter, Photo Voltaic, Ripple voltage.

I. INTRODUCTION

The changes of rising oil costs and progressively stressing level of contamination appeared differently in relation to the new arrangements of feasible improvement to make elective and sustainable power sources more alluring. Financial motivators and gigantic progression in electronic innovation advance the utilization of PV frameworks. These frameworks show a straightforward and advantageous arrangement from a financial perspective. The utilization of a converter on these photovoltaic frameworks is much additionally convincing as it builds their effectiveness and diminishes their expenses. Though, the reduced voltage level of these non-conventional energy skills requires for high efficacy heavy boost up [1]. Hypothetically, increased source level ratio could be acquired by the ordinary models, for example, voltage-lift up sort and step-up mode converters with large duty ratio [2]. Many high boosts up voltage converters are proposed to raise the voltage ratio and efficacy of the model which is categorized in to three zones [3–9].

Parallel organized arrangement of VMCs is implemented to improve the source voltage ratio limit in a stretchy path[10]. The voltage sources of all storage along the VMCs are similar through raises the elasticity of the model. An IDBS mode converter is projected as a large step-up mode power converter circuit [11]. Variant and categorization of tapping converters are represented in [12]. Parallel and stacked mode inductive coupler step up mode converters have been designed in [13-15], correspondingly. This designs converters are ease and price reasonable with only single-active control.. The authors in [16-17], ought to incorporated a waveform of a passive and a active diode hooked on the positioning the converter [20].

In [18], two ways waveform are located on together. By incorporation of HFCI and waveform in sequence mode with the switch, aeasy high voltage ratio DC–DC in [19].The single switch sepic converter with VM has existed in [21].The model design in [22], involves the CI, voltage-lift technique circuit mode and the clamping mode circuit. The model in [23] is shaped by paralleling a usual boost type model and a CI boost mode by contributing the switch. This model character not only reduces ripple current, likewise quadratic- gain ratio of the converter. However, due to parallel working of this design, the efficacy is not promised.

A single active switch sort, huge step-up mode model depending on swapped model CI and switched model storage device has been accessible in [24]. Then massive input side filters must be utilized to sieve out the noise filling of input current. By the way, working, the power compactness and renovation efficacy is reduced at peak power range. In huge power applications, research analyst have been pointed on inter-leaved type mode converters owing to the merits which are propose, such as reduced input source-current, huge power compactness and huge efficacy [25-27].On relying the above considerations, this manuscript details a novel non-isolated modified multilevel sepic converter. The PV conversion block is illustrated in Fig 1. Here the recommended converter is the combination sepic converter and voltage tripler circuit. It helps it attaining good static gain with suitable duty ratio and better efficiency. Overall, the proposed model converter full fills the following needs in PV energy transformation schemes: Higher voltage gain conversion ratio, reduced voltage strain athwart semiconductors, Recycling of inductive leakage energy, Lessening of reverse recovery diode current problems, Lessened input ripple current and high conversion rate efficacy.

Fig.1 PV energy conversion

The manuscript is prearranged as below. In section 2, the operation of the designed model in CCM is explained. In section 3 the design and examination of the projected converter is explained. In section 4 Comparative examination of projected converter with conventional model is explained. In section 5 investigational fallouts are evaluated. Conclusion is followed by section 6.

II.OPERATION OF THE PROPOSED CONVERTER

The projected circuit is represented in Fig 2. Few assumptions are made to streamline the circuit designs and operation of the projected converter.

1) The converter functions under CCM at the stable condition.
2) Semiconductor strategies are considered as ideal in nature.
3) The capacitor utilized has high storage voltage and hence the capacitors are expected to be constant. Hence the input capacitor and the output capacitor are considered as equal.

The design consists of main switch S_1, inductors L_1, L_2, diodes D_1,D_2,D_3,D_4, D_5*and* D_6 , capacitors$C_1, C_2, C_3, C_4, C_5$and output capacitor C_6. The VT is united with basic sepic to progress the voltage improvement level of the converter. The switching limit in the semiconductor device is reduced. Capacitors operate as similar operation in conventional boost converter.

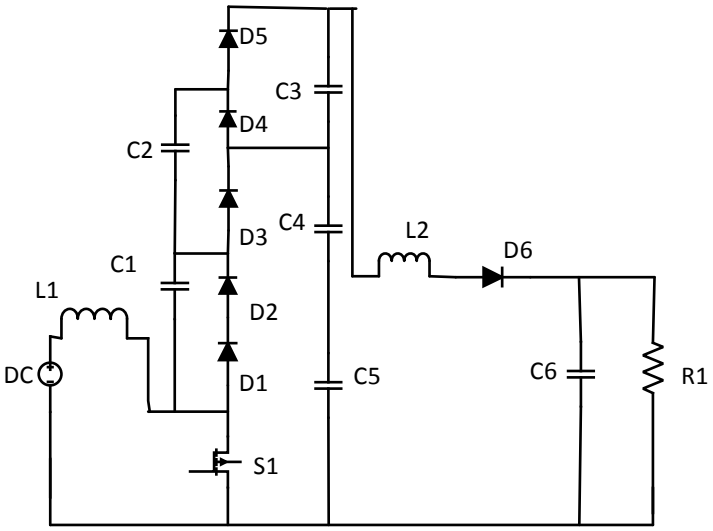

Fig.2 Proposed single switch Converter

2.1. Continuous conduction mode operation:

The proposed converter functions in two manners. The modes of operations are shown in Fig.3 and Fig.4

Mode I [t0–t1]: When the switch S_1 is crooked-on diodesD_2,$D_4$and D_6 is turned ON. Diode D_1, D_3andD_5 are reverse biased. The voltage V_{in} is delivered to L_1 and $V_{C3} - V_{C2} - V_{C1}$ is delivered to L_2. These inductors help in storing the energy. The C_0ejects the required liveliness to the load for its operation. When the switch turns off, this mode tops. Also the diodeD_3 and D_0 current attains zero at t=t_1.

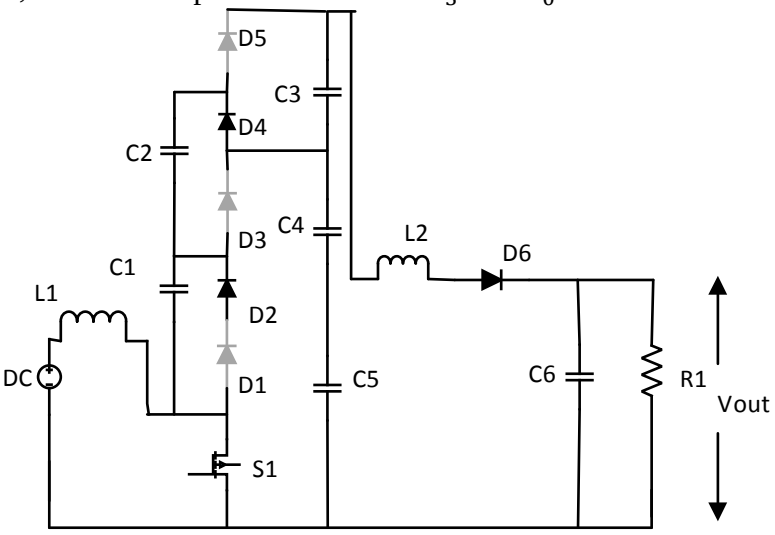

Fig.3. Proposed DC-DC converters turn on mode

Mode II [t1–t2]: When the S_2, is bowed OFF, the diodes D_2 and D_4 are in OFF condition. The diodes D_1,, D_3 and D_5 are in forward condition. The capacitors are charged by the inductor L_1 and L_2. The load receives the energy by discharging mode of the capacitor. This operation ends when Switch is crooked ON. The subsequent cycle continues.

The main operational waveform is represented in Fig.5. The total capacitive voltage is identical to the production voltage of the model.

$$V_o = V_{C3} + V_{C4} + V_{C5} + V_{C6} \quad (1)$$

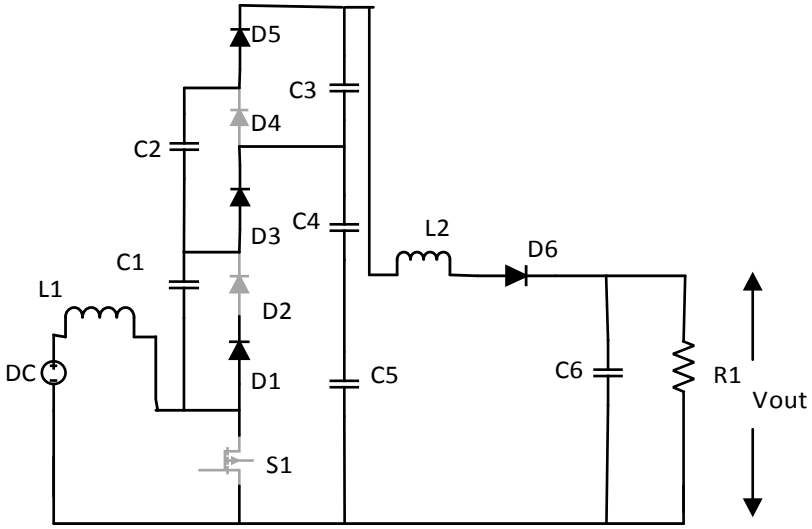

Fig.4 Proposed DC-DC converters turn off mode

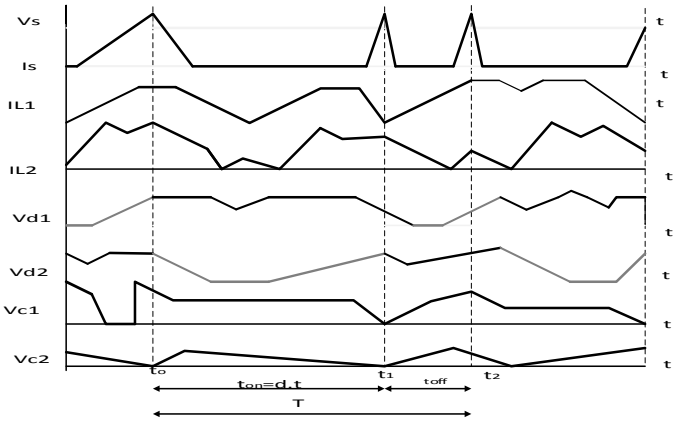

Fig. 5.CCM operation waveforms

III.ANALYSIS OF THE PROPOSED CONVERTER

Here,the theoretical analysis of the designed model is explained by following with design procedural of the converter proposed.

3.1 Static gain and switching voltage analysis:

At steady condition, the inductance value is considered as null and the equation is termed as below and hence in CCM operation, the inductor L_1 is given as

$$V_{in}\,d = V_{C6} - 3V_{in}(1-D) \quad (3)$$

Here *d* is duty cycle, input voltage is V_{in} .On rearranging the values in Eq. (3), and the capacitor C_0 value is obtained same as static gain..

$$V_{C6} = \frac{3V_{in}}{1-D} \quad (4)$$

The inductor L_2 is zero at steady state condition,

$$(V_{C6} - V_{C1})D = (V_0 - V_{C6})(1-D) \quad (5)$$

From equation 1, capacitor 1 voltage is given by,

$$V_{C1} = V_0 - V_{C2} - V_{C3} - V_{C6} \quad (6)$$

By substituting the equation 3 & 4 in 5 the static gain is derived as ,

$$\frac{V_0}{3V_{in}} = \frac{(1+D)}{(1-D)} \quad (7)$$

The duty cycle equation of the converter proposed is given as,

$$\frac{1-D}{1+D} = \frac{3V_{in}}{V_0} \quad (8)$$

The capacitor voltage in C_2, C_3 are given as

$$V_{C2} = \frac{D.3V_{in}}{1-D} \quad (9)$$

$$V_s = \frac{3\times V_{in}}{1-D} \quad (10)$$

The output voltage of the proposed model is given as,

$$V_0 = \frac{D\times 3V_{in}}{1-D} \quad (11)$$

On taking the diode voltage drop in to account,

$$V_0 + V_d = \frac{D\times 3V_{in}}{1-D} \quad (12)$$

On simplifying,

$$D = 1 - \frac{nV_{in}}{V_0} \quad (13)$$

The attained duty cycle is 0.775.

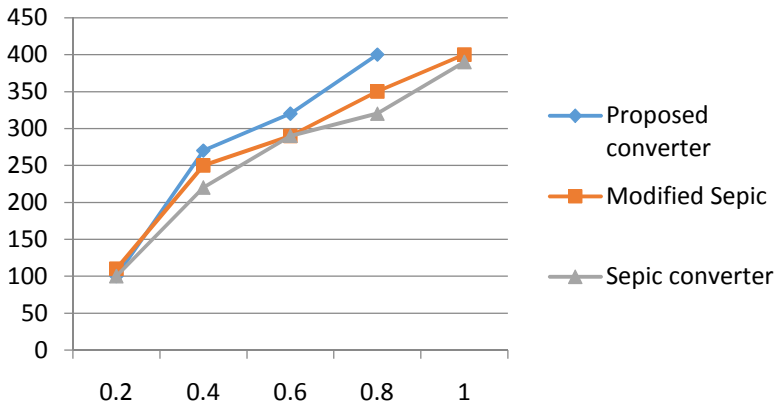

Fig.6 Converter output voltage

On comparing the proposed converter with conventional converter, the step up of voltage range is high. The comparison chart depending on output voltage is depicted in Fig.6.

IV.RESULTS AND ANALYSIS

In proposed converter output voltage ripple level is much small and the steady state is attained at earliest. The maximum over shoot is 0% and the transient response analysis is better than multilevel sepic converter. The output voltage is reliable and hence switching operation is good with reduced conduction loss and switching loss. The inductive voltage occurs only in positive value. From the fig.13, the output voltage attained from planned converter is less in ripple, the maximum over shoot is 0%, the settling period is 0.5ms and the stable state error is 0.6%. This output signifies that the converter operates in stable state. The transient analysis comparison is depicted in Table.2 .In fig. 13current output and voltage source of projectedmodel is depicted. There it can be noted that the current is unrestricted from disturbances and it is constant which helps the converter to be steady state manner. The output ripple is less which provides the best performance of the plannedmodel. The parameter of the designedmodel is demonstrated in Table 1. Hence these converter well suits for PV applications and it boost up the PV voltage to the application level.

Table 1 Proposed Converter parameters

Components	Parameter
Input voltage	30 V
Output voltage	400 V
Input current	15.2 A
Output current	1 A
Inductor L_1, L_2	205, 180 µH
Capacitor C_1, C_2, C_4	2.2µF
Capacitor C_3	2.2µF
Capacitor C_0	40 µF
Resistor	400 Ω

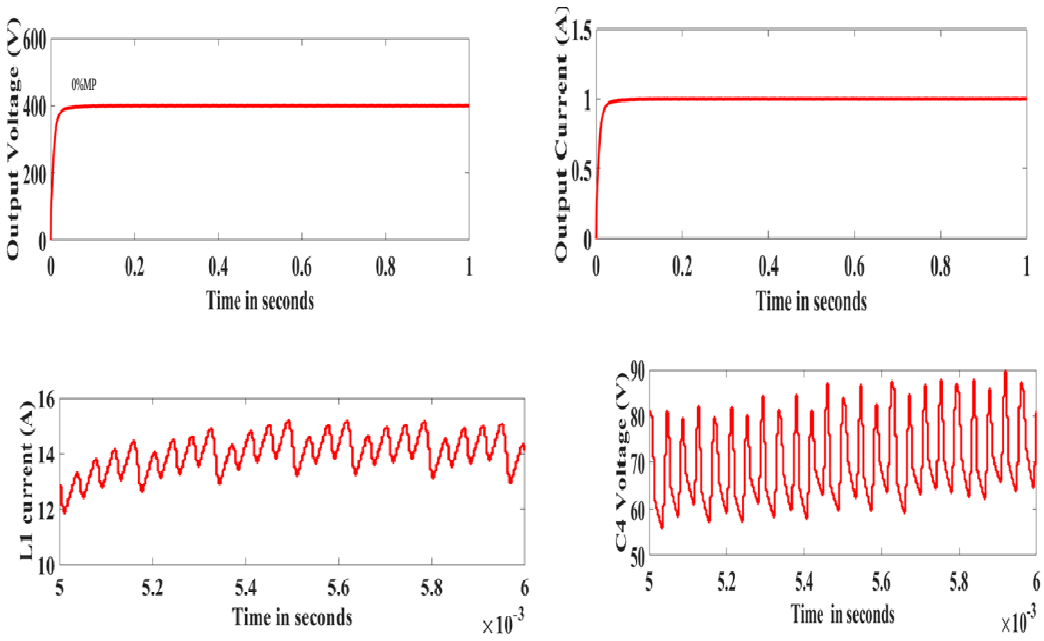

Fig 13.simulation waveform of output voltage, output current, inductive current and capacitive voltage of proposed converter (proposed converter)

Table 2Transient Response Analysis

Transient response	Multilevel Sepic Converter	Proposed Converter
Settling time	0.5 ms	0.15 ms
Peak time	0.08 ms	0.03 ms
Rise time	0.06 ms	0.014 ms
Maximum overshoot	5%	0%
Steady state error	1.6%	0.25 or 0.6%

V.CONCLUSION

In this manuscript a step up voltage gain modified multilevel sepic converter has been proposed. The working and function of the designedcircuit in model mode is elucidated. The operation of the design is detailed by the waveform depiction. The proposed model attains high static gain with reduce switching and conduction loss. The concept of VT has been embedded to improve the boosting of voltage ratio with efficiency. The steady state and design analysis has been explained. The simulation scrutiny of the projected converter is accessible clearly on comparing with multilevel sepic converter results. The transient comebackinvestigation of the designedmodel is elucidated. A model has been established in laboratory and confirmed the working of converter. The investigational results prove that the projected converter attains high stepping of voltage with tripling of voltage level with an efficiency of 94% with reduced switching stress.

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