A Fuzzy Controlled Zeta DC-DC Converter for PV Based Applications

T.Arunkumari[a], V.Indragandhi[b], R.Raja Singh[c]
[abc]Department of Energy and Power Electronics, School of Electrical Engineering, VIT Vellore, India.

Abstract

In this manuscript a zeta converter with extreme voltage ratio module is proposed. The projected converter has the feature of stable frequency and output even though disturbance occurs. It also achieves high static voltage, high efficacy, low voltage strain and less switching loss. The voltage doubler technique is implemented in the designed converter. With reduced duty cycle the high voltage conversion is achieved. The proposed zeta converter is controlled by fuzzy controlled technique. The function of the power converter underneath Continuous Conduction Mode (CCM) is explained. The input of 30 V is boosted up to 220 V. The simulation of the proposed model is done with MATLAB Simulink.

KEYWORDS: Continuous Conduction Mode, Duty Cycle, Fuzzy Controller, High Voltage Conversion, Switching loss.

I.INTRODUCTION

The usage of natural source such as Photo Voltaic (PV) has been raised sequentially, due to global warming and the demand of fossil fuels. PV scheme sutilize the solar vitality to harvest electrical energy. On the other hand, the produced DC source voltage by a PV scheme is very less. To handle this downside, converters develop a significant section of natural source [1-3]. Hence, different DC converters through extreme voltage conversion ensure been projected for solar schemes. Conventional converter was utilized for high voltage conversion with limited duty range. Due to occurrence of the high losses in active and passive, the efficacy and the static gain are restricted [4, 5].

To exceed the limits, several DC models such as the IBC [6], soft-switching mode [7], coupled-inductive schemes [8] and VM technique [9-12] designed which is capable to deliver extreme static gain. It is perceptible that other schemes converter depends on the mixture of this topography in current years [13-17]. Amongst these design each has their own merits and de-merits.

Many techniques have been implemented for high voltage conversion technique such as inductive coupling method, switched capacitor method, voltage doubler method and voltage multiplier techniques. All the above methods have advantages and disadvantages. The common drawbacks in all those techniques are the size of the system is increased. Recently, various VMC design have been offered in [10-12]. A new VMC structure has been projected in [10]. A new scheme of VM has been presented in [11-12]. It is essential to remind that the source current of designed models in is sporadic and it is a limitation. Also, the static gain of this topography is stable and cannot be synchronized. Hence, these cannot be exploited in PV schemes due to their restriction to follow the MPP. Then voltage lift technique has been proposed and it is implemented for boost converter [18-20]. In this paper the voltage lift technique is implemented for zeta converter. The model is depicted in Fig.1

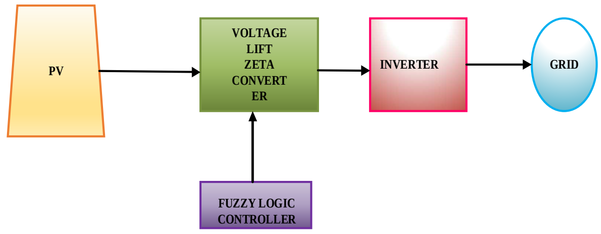

Fig.1 Overview of conversion system

Here the manuscript contains, a new voltage lift dc converter with PV is projected which can over a wed the exceeding stated limitations of the conventional converters. In section II the function of the designed model in CCM mode is explained. In section III the analysis of the proposed model is detailed. Section IV deals with converter control fuzzy logic. In section V simulation results are explained. Section VI is followed with conclusion.

II. OPERATION OF THE PROPOSED CONVERTER

The designed model is depicted in the Fig. 2. Few conventions are made to streamline the circuit designs and operation of the projected circuit.

1) The proposed circuit operates under CCM at the stable state condition.
2) Semiconductor strategies are considered as ideal in nature.
3) The capacitor utilized has high storage voltage and hence the capacitors are assumed to be constant. Hence the input capacitor and the output capacitor are considered as equal.

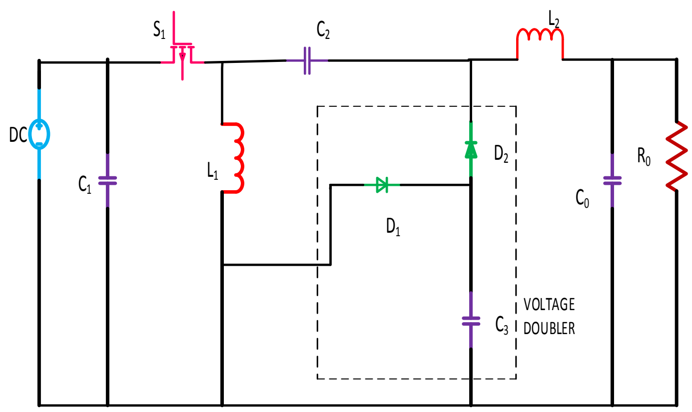

Fig.2 proposed converter

2.1 Continuous conduction mode:

The proposed converter conducts in two modes. They are switch off and switch on mode. They turn on and turn off modes are portrayed in Fig. 3 and Fig.4

Mode I [t_0-t_1]: When the S_1 switch, is crooked ON, diode D_1 and D_2 is crooked ON. The voltage V_{in} is delivered to L_1 and $V_{C3} - V_{C2} - V_{C1}$ is delivered toL_2. These inductors help in storing the energy. The Output capacitor C_0 discharges the obligatory energy to the capacity for its operation. When the Mosfet switch off, this mode ends.

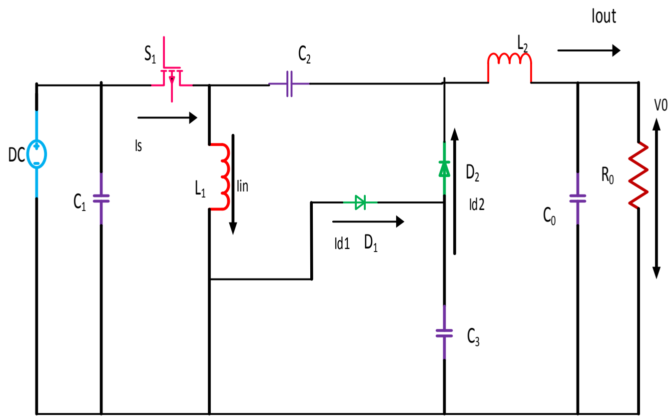

Fig.3 Turn On mode of proposed converter

Mode II [t_1-t_2]: When the S_2, is crooked OFF, the diodes D_1 and D_2 are in OFF condition. The capacitors are indicted by the inductor L1 and L2. The load receives the energy by discharging mode of the capacitor. This operation tops when Mosfet is crooked ON. The next cycle continues.

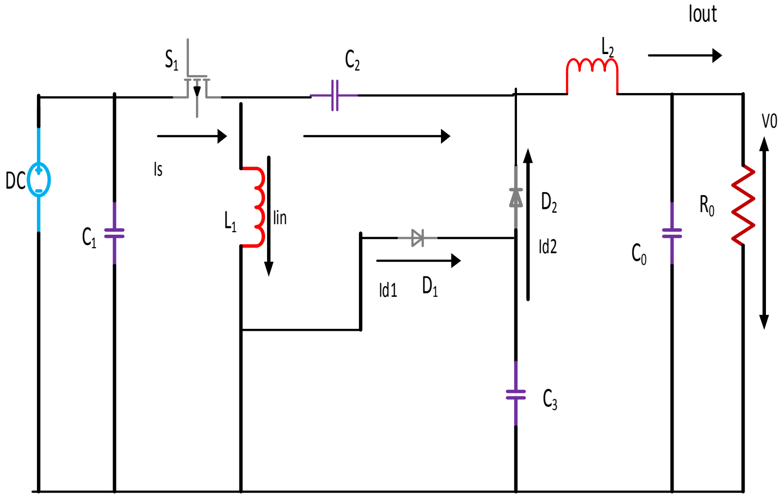

Fig.4 Turn Off mode of proposed converter

The keyactive waveform is characterized in Fig. 5. The total capacitive voltage is equivalent as voltage at output terminal of the model.

$$V_o = V_{C1} + V_{C2} + V_{C3} + V_{C0} \qquad (1)$$

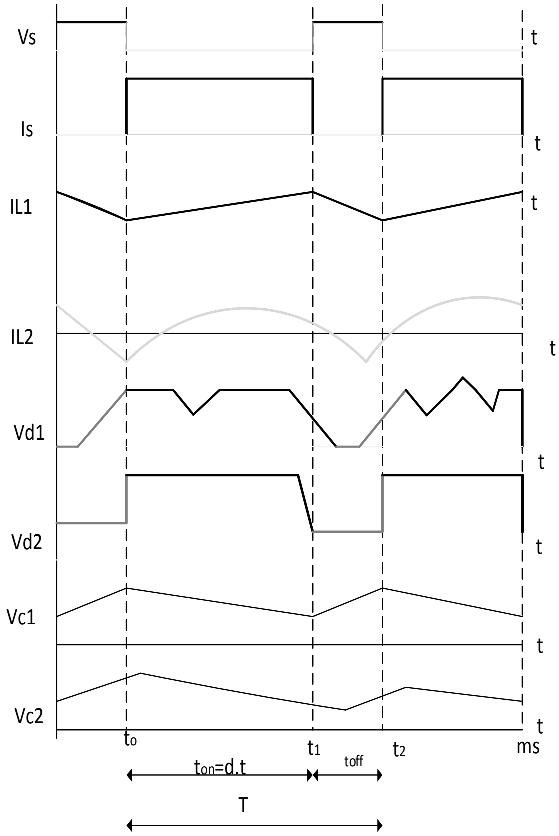

Fig.5 operational waveform

III ANALYSIS OF THE PROPOSED CONVERTER:

In this section the examination of the model is derived. The parameter values of the inductor and capacitor is analysed. The voltage gain and duty cycle are calculated in this section.

3.1 Calculation for Voltage gain :

In the stable state, the normal voltage crosswise inductor L is zero. Thus

$$V_{cs} = V_{in} \quad (2)$$

During ON condition, the voltage thruC_1 is identical to the voltage acrossC_s. SinceC_s, and $C_1$are sufficiently large,

$$V_{c1} = V_{cs} = V_{in} \quad (3)$$

The inductor currentI_l, upsurges thru switch on time and drops thru switching off period. The voltage transferral gain of lift circuit is given as,

$$M_s = \frac{V_0}{V_{in}} = \frac{1}{(1-D)} \quad (4)$$

From here we can attain,

$$I_{in} = I_L = \left(\frac{1}{1-D}\right) I_0 \quad (5)$$

The converter output voltage is given by,

$$V_0 = \frac{D}{1-D} * V_{in} \qquad (6)$$

As utilizing the voltage doubler, the converter gain is given as

$$V_0 = \frac{2D}{1-D} * V_{in} \qquad (7)$$

3.2 Duty cycle calculation:

The proposed converters of voltage varies due to the duty cycle control. And also it is dependent on elements in the circuit. The output of the designed converter is given as,

$$D = \frac{V_{out}}{(2V_{in} + V_{out})} \qquad (8)$$

$$\frac{D}{1-D} = \frac{V_{out}}{2V_{in}} \qquad (9)$$

3.3 Inductor Selection:

The inductance values are identified with the help of input current ripples i.e.$\Delta I_{L1} and \Delta I_{L2}$.

$$L_1 = \frac{D*2v_{in}}{f.\Delta I_{L1}} \qquad (10)$$

$$L_2 = \frac{1-(D*v_{c2})}{f.\Delta I_{L2}} \qquad (11)$$

$$I_{ripple} = I_{out} \times \frac{V_{out}}{2v_{in}} \times 40\% \qquad (12)$$

3.4 Capacitor Selection:

Voltage ripple (Δv_c) is used to calculate the capacitance value. The ripple value is obtained by the 10% of the input voltage value. The capacitive ripple current is obtained using eq.14 and the ripple current is 0.113 A. The formula to obtain the capacitor value is given by,

$$c_1 = c_2 = c_3 = \frac{I_0}{f.\Delta v_c} \qquad (13)$$

The ripple voltage is obtained by,

$$\Delta v_c = \frac{v_{in}}{1-d} * 10\% \qquad (14)$$

The ripple capacitive current is attained by,

$$I_{cs} = I_0 \times \sqrt{\frac{V_0}{3V_{in}}} \qquad (15)$$

3.5 Output capacitor:

The output capacitor c_0 is designed as same as boost converter design. To calculate the output capacitor frequencyf_c, output powerp_0, output voltage v_0 and output ripple voltageΔv_0. 1% of output voltage is equivalent to production ripple voltage. The capacitance is calculated using

$$c_0 = \frac{p_0}{4\pi f_g v_0 \Delta v_0} \qquad (16)$$

Component stress:

The component design purpose the switch current i_1 and i_2 at the turn ON and end of turn ON is found using below equation. On taking the theoretical efficiency value94 % . Here the RMS current of the switch (i_{rms}). The comparison is of the converter is detailed in table 1.

$$\mathrm{i_1} = \left(\frac{\mathrm{p_0}}{\eta * \mathrm{v_{in}}} - \frac{\Delta \mathrm{I_L}}{2}\right) + \left(\mathrm{i_0} - \frac{\Delta \mathrm{I_L}}{2}\right) \qquad (17)$$

$$\mathrm{i_2} = \left(\frac{\mathrm{p_0}}{\eta * \mathrm{v_{in}}} + \frac{\Delta \mathrm{I_L}}{2}\right) + \left(\mathrm{i_0} + \frac{\Delta \mathrm{I_L}}{2}\right) \qquad (18)$$

$$\mathrm{i_{rms}} = \sqrt{\frac{1}{3}.(\mathrm{i_1^2} + \mathrm{i_1^2} + \mathrm{i_1}.\mathrm{i_2}).\mathrm{d}} \qquad (19)$$

The output current($\mathrm{i_0}$) is same as diode current$\mathrm{i_{D1}}$,$\mathrm{i_{D2}}$ and$\mathrm{i_{D0}}$

$$\mathrm{i_0} = \mathrm{i_{D1}} = \mathrm{i_{D1}} = \mathrm{i_{D1}} = \frac{\mathrm{p_0}}{\mathrm{v_0}} \qquad (20)$$

Table 1-Evaluation of the designed converter and conventional zeta converter:

Parameters	Zeta converter	Proposed topology
Input current	**discontinuous**	**constant**
Number of switches	**1**	**1**
Capability of usage of PV	**no**	**yes**
Cost	**low**	**average**
Output voltage	**constant**	**variable**
Voltage gain	$\mathbf{V_0 = \frac{D}{1-D} \times V_{in}}$	$\mathbf{V_0 = \frac{2D}{1-D} \times V_{in}}$
Ripple voltage	**>3**	**0.75**
Ripple current	**-**	**0.113**

IV. FUZZY LOGIC CONTROLLER

Fuzzy-Logic Controller (FLC) is one of the most booming applications of fuzzy theory, implemented by Zadeh in 1965 [2]. Its best features are the usage of linguistic variables relatively than numerical contents. Linguistic variables are utilized as normal variables are such as small and large, which is represented as fuzzy sets. It is an addition of a crisp set which exhibits the membership or non-member ship function. Fuzzy sets permits specific function which defines that an element may belong or may not belong to the set.

The FLC is utilized to control the zeta converter operation. This fuzzy is utilized for any other control operation. The main concept of fuzzy is the rules. The rules should be defined first according to the converter operation. Here in this design, the error values are given as input to the fuzzy converter. The change in error is created by delay unit. The fuzzy output is compared with relational operator and it is given to the gate of the MOSFET. The fuzzy block is depicted in Fig. 6

FLC consists of three main blocks namely fuzzification, FIS and defuzzification. In first process the data is converted to linguistic variable. There are two methods they are, Mamdani and Sugeno. Scheme of membership function shown in Fig.7, Fig.8 and Fig.9 respectively. To attain crunchy output diverse defuzzification approaches can be utilized e.g., centre of gravity. Rule base and data base are given to decision making. The converter rules for fuzzy controller is depicted in Table. 2 and surface plot is represented in Fig.10

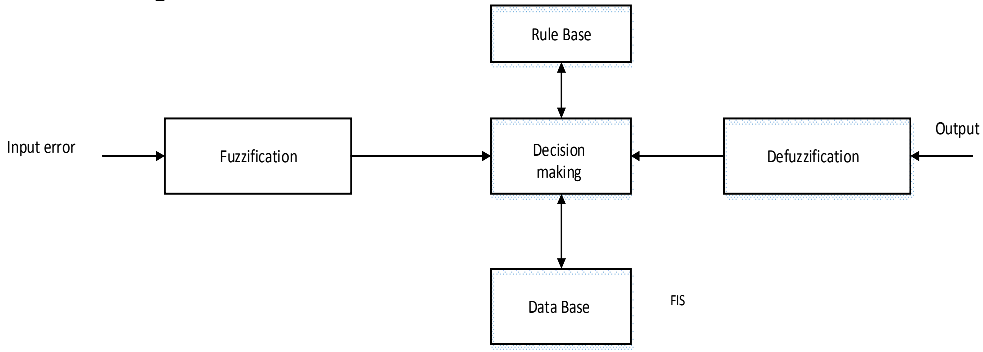

Fig.6 Fuzzy Block

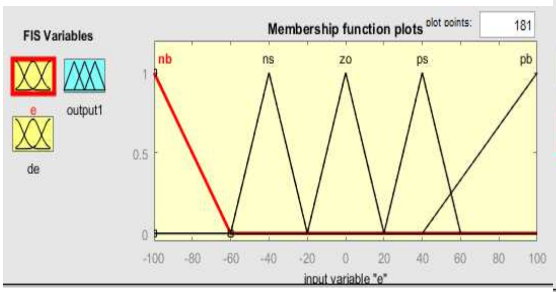

Fig.7 Input error membership

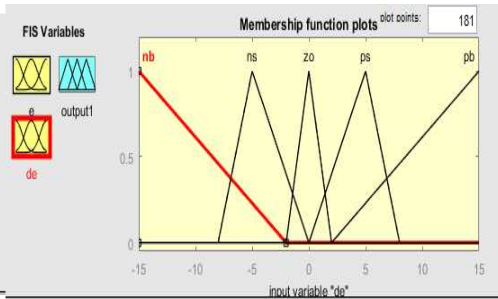

Fig.8 Input change in error membership

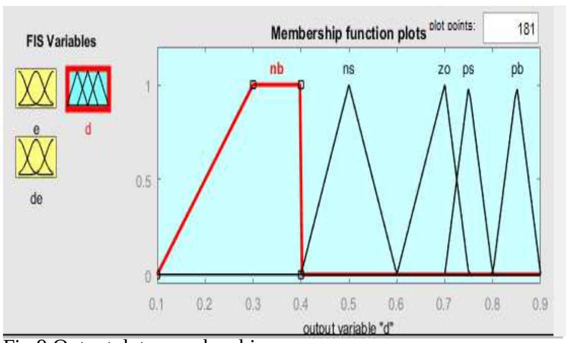

Fig.9 Output duty membership

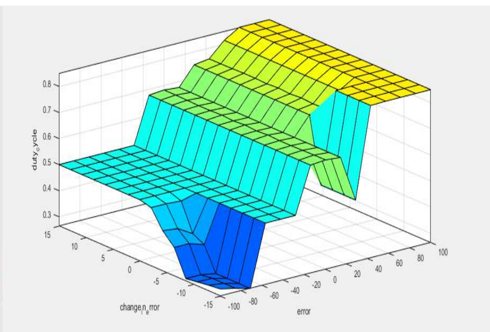

Fig.10 Surface plot of fuzzy

Table:2-Fuzzy Rule for proposed converter

ERR	NB	NS	Z0	PS	PB
NB	nb	ns	ns	ns	ns
NS	ns	ns	ns	ns	ns
Z0	zo	zo	zo	zo	zo
PS	ps	ps	ps	ps	ps
PB	pb	pb	pb	pb	pb

V. SIMULATION RESULTS

The zeta converter with voltage lift technique proposed is tested with Matlab Simulink. The 30 V input is enhanced up to 170 V. The key benefit of the designed converter is its one switch, condensed size, increased efficiency, less duty cycle, high voltage boost up with reduced ripple value. The generated voltage and current consequences are portrayed in the Fig. 11 &Fig 15. The ripple and peak over values are reduced. The enactment of the converter is better associated to other zeta converters. The waveforms of other components are depicted from the Fig.12-14. The converter parameters are represented in Table.3

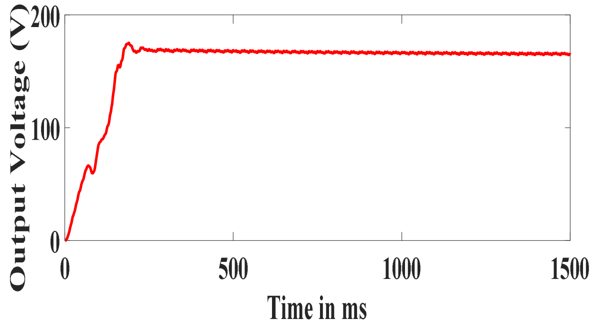

Fig.11 Output voltage

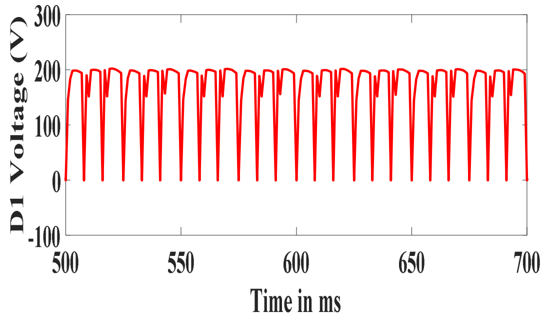

Fig.12 Diode 1 voltage

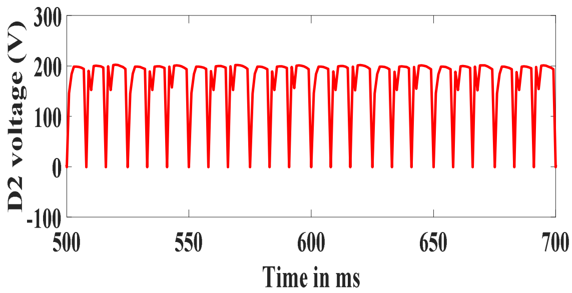

Fig.13 Diode 2 voltage

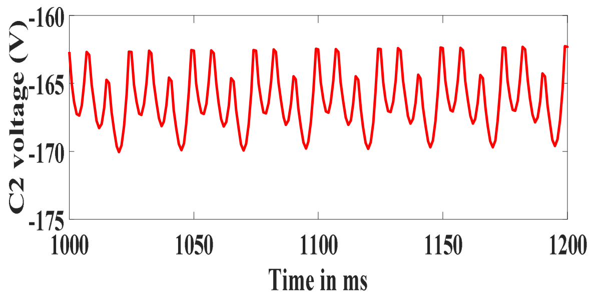

Fig.14 Capacitor 2 voltage

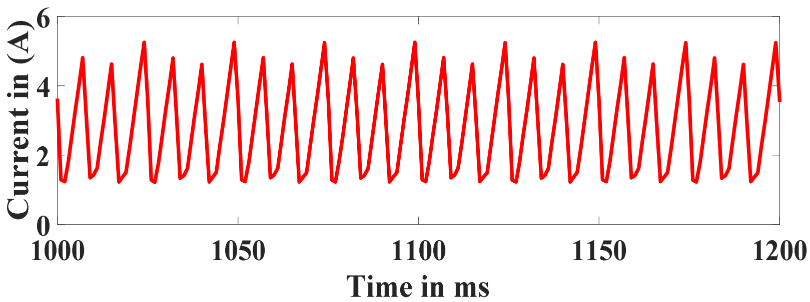

Fig.15Inductor 1 current

Table:2-converter parameters:

Components	Parameter
Input power	30 V
Output power	170 V
Input current	5 A
Output current	0.5 A
Inductor L_1, L_2	205e-6, 180e-6 μH
Capacitor C_1, C_2	$2.2e^{-6}$ μF
Capacitor C_0	$40e^{-6}$ μF
Resistor	400 Ω

VI.CONCLUSION

Here, a voltage doublerzeta converter is proposed. The CCM mode operation is explained in detail with the waveform. The mathematical expression for the projected converter is derived and analysed through the simulation results. Also the designed converter is associated with conventional Zeta converter in the basis of ripple, efficiency and gain. In this designed converter the duty limit attained is 0.73 and the ripple source current is reduced to 0.113 A. The main advantage such as reduced size of the converter, reduced number of switch, reduced ripple current is attained. This converter has high efficiency while switching and conduction loss is less. The efficiency attained is stable on comparing to other converters. This converter is suitable for PV energy conversion and it is also suitable to connect to the inverter source. This can be analysed through hardware results in future.

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